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► **To cite this version:**

Khadija Hamidoun, Rahmad Sadli, Yassin El Hillali, Raja Ellassali, Atika Rivenq, et al.. Implementation of a New IR-UWB System Based on M-OAM Modulation on FPGA Component. International Journal of Wireless and Mobile Networks, 2018, 10 (2), pp.01-17. 10.5121/ijwmn.2018.10201 . hal-03578085

HAL Id: hal-03578085

<https://uphf.hal.science/hal-03578085>

Submitted on 30 May 2024

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IMPLEMENTATION OF A NEW IR-UWB SYSTEM BASED ON M-OAM MODULATION ON FPGA COMPONENT

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ABSTRACT

This paper presents the implementation of an Impulse Radio Ultra Wide Band (IR-UWB) communication system based on Orthogonal Amplitude Modulation (OAM) on the FPGA board (Field Programmable Gate Array). The Orthogonal Amplitude Modulation is a new modulation technique that provides a high data rate transmission, using the orthogonal waveforms named MGF (Modified Gegenbauer Function). In this work, the FPGA card and the converters DAC (Digital-to-Analog Converter) and ADC (Analog to Digital Converter) are considered to perform the implementation. The system is running in the simulation field and in the real system on the hardware equipment. The obtained results show that the implementation of UWB-OAM system on FPGA board is running well and provide a high - real time computations system.

KEYWORDS

UWB, FPGA, OAM, ADC, DAC, simulation, real time system

1. INTRODUCTION

The Ultra Wide Band (UWB) is a promising technology which has several advantages such as low power transmission, high data rates, low-cost, immunity to multi-path propagation, less complex transceiver hardware, secure communication and low interference [1], [2], [3].

Originally, UWB is designed for radar systems, but now it is also used for communication and positioning applications. In 2002, the Federal Communications Commission (FCC) approved the unlicensed frequency band between 3.1 GHz and 10.6 GHz for indoor UWB wireless communication systems [4]. FCC defined the UWB as any wireless transmission scheme that occupies more than 500 MHz of absolute bandwidth. Moreover all system, whose fractional band $BW=f_c$ is greater than or equal to 20% is also considered as UWB systems. Where BW is the transmission bandwidth and f_c is the central frequency.

In our work, communication for Intelligent Transportation systems, especially V2I (Vehicle / Infrastructure) or V2V (Vehicle / Vehicle), is considered [5]. Such applications require high transmission data rate and high level of security and quality of service (QoS). For this purpose, M-OAM modulation is considered [6], [7].

It is a new modulation technique that provides a high data rate transmission, based on orthogonal waveforms [8]. Thus, the objective of this paper is the simulation and implementation of our M-OAM UWB communication system proposed previously in [6], [7], [8].

In order to process the UWB waveforms and achieve a high-speed data rate, the use of a very high sampling rate device and massively parallel computation processor is required. Consequently, the Xilinx FPGA Virtex-5, the DAC and ADC S4/3G converters are considered [11], [12]. The system is developed using VHDL (VHSIC Hardware Description Language).

In this paper, we focus on developing a complete prototype for M-OAM UWB system. For transmission, we generate the signal to be transmitted and apply Orthogonal Amplitude Modulation (OAM) using FPGA and DAC Cards. Then, the reception consists of ADC data captured, parallel correlation, peak detection, synchronization and decoding process.

The principle of the system is that the transmitted signal is firstly coded in 4-OAM modulation. Then, this data is transmitted by an UWB antenna. The reception UWB antenna captures these signals and a high speed ADC sends to the input of the FPGA board 16 parallel samples at every clock cycle. These signals are used in order to perform the parallel correlation with the reference signal, stored in the FPGA memory. Thus, the result can be decoded by finding the peak of the correlation and so it can be transferred to the host application as a valid data received.

This paper is organized as follows. In the first section, we present the literature review of M-OAM modulations, FPGA board, DAC and ADC converters. The second section presents the system performances given by the simulation. In the latter, we focus on the design of the proposed system and present the simulation results provided by ISE Project Navigator ver.14.6 and ISIM ver.14.6. The third section is dedicated to the system implementation and corresponding results. Finally, a conclusion is drawn from perspectives.

2. LITERATURE REVIEW

2.1 Orthogonal Amplitude Modulation (M-OAM)

M-OAM is a new modulation technique proposed previously in [6], [7], [8]. This new modulation is inspired by M-QAM (Quadrature amplitude modulation), where M is a number of states. M-OAM modulations are designed for IR-UWB systems, where no carrier could be used. Therefore, the idea is to replace the carrier used in M-QAM modulation by orthogonal waveforms. MGF (modified Gegenbauer functions) are the orthogonal waveforms considered in our work [9]. The first 4 orders of MGF functions are defined in the following equations and presented in Figure 1:

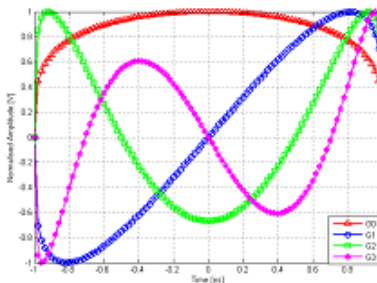


Figure 1. Time presentation of Gegenbauer polynomials

The concept of M-OAM modulations is to modulate the transmitted pulse in M states. M is a multiple of 2, $M = 2^n$ when n is the number of bit per symbol. Incrementing n increases the number of transmitted bits per symbol and hence the data rate. Depending on the value of n, three cases of M-OAM modulation are proposed: 4-OAM, 16-OAM and 64-OAM; as well as the particular cases 8-OAM and 32-OAM with odd values of n [6], [7].

This modulation technique offers a very high data rate and is robust against the propagation channel effects. This modulation multiplies the data rate of conventional UWB system by a factor of n $D_{M-OAM} = n * D_{conventional}$ as illustrated in table 1:

Table1. Data rate of each M-OAM modulation, where D is the data rate of conventional UWB system

n	M states	Modulation	Data rate
2	4	4-OAM	2D
3	8	8-OAM	3D
4	16	16-OAM	4D
5	32	32-OAM	5D
6	64	64-OAM	6D

The principle of 4-OAM modulation is to transmit 2 bits=symbol and then the data rate is doubled [10]. The information of the first bit presents the position of the pulse as the PPM modulation (Pulse Position Modulation). The second bit presents the polarity of the pulse as the bipolar modulation. So, there are four possible combinations of MGF pulse (Cf Figure 2). In 4-OAM modulation, only one MGF order is used. Then for the other M-OAM cases, we use more MGF waveforms: two for 16-OAM and three for 64-OAM modulation.

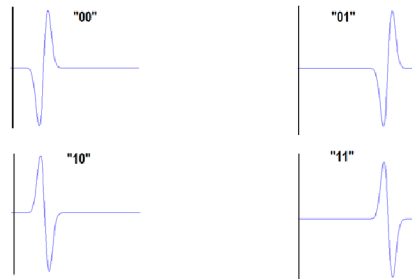


Figure 2. Symbols of 4-OAM modulation

2.2 FPGA

Field Programmable Gate Arrays (FPGAs) are semiconductor devices, based on a matrix of configurable logic blocks (CLBs). The FPGA board provides high speed, high level of integration, high flexibility, and low development costs.

FPGAs are very useful for operations that process large data streams, such as digital signal processing and networking. In comparison with the microprocessor, FPGA can be faster hundreds of times because it implements parallel spatial computations and simultaneously computes millions of operations in resources distributed across a silicon chip [11]. The other benefit of FPGA is that it can be programmed and reprogrammed many times to meet the desired application or functionality requirements after manufacturing.

2.2.1 Xilinx FPGA Board

The ADM-XRC-5T1 is an FPGA card from Alpha-Data which has a high-performance PCI Mezzanine Card (PMC). It is designed for applications using Virtex-5 FPGAs from Xilinx. This card communicates with the computer using a PCI bridge developed by Alpha-Data which supports PCI-X and PCI. Thus, a high speed multiplexed address/data bus connects the computer to the FPGA [12]. This card also uses a Primary XMC connector to provide high-speed serial connections. Figure 3 shows the physical board of ADM-XRC-5T1 card.



Figure 3. ADM-XRC-5T1 Board

2.3 Digital to analog converter (DAC)

XRM-DAC-D4/1G is a DAC card from Alpha-Data which has sampling rate up to 1 GHz [13]. Digital to analogue conversion plays the significant role in mixed analogue and digital systems. In modern Digital Signal Processing (DSP) solutions, where high - speed signal are employed, the request of using high-speed DAC is increasing. Figure 4 describes the DAC board layout.

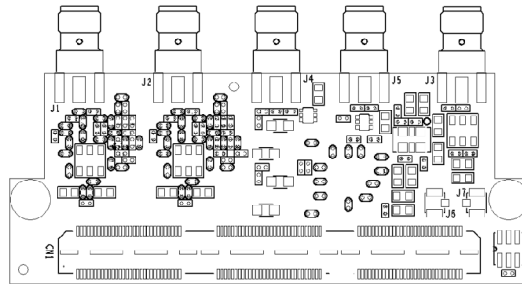


Figure 4. XRM-DAC-D4/1G Board

J1 I channel DAC output, J2 Q channel DAC output, J3 External Clock Input, J4 Aux IO connector, J5 Trig IO connector, J6 GPIO connector, p side, J7 GPIO connector, n side.

The application must first configure the FPGA with the bit stream using the SDK standard. The various system blocks must be configured in the correct sequence in order to generate analogue signals correctly [14]. The clock source must be established, the synthesizer and the generation circuit FPGA clock configured.

Once a stable DCLK signal has been established, the DAC internal registers can be configured to suit the required operating frequency.

2.4 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is the front end component in the UWB receiver. In this project, the S4=3G ADC card from Alpha-data is considered.

This card uses the ADC083000 from the National Instruments. It is an 8 bits resolution ADC at sampling rates up to 3:4 GSPS. It consumes low power and high - performance CMOS analog to digital converter [15].

3. DESIGN OF THE UWB-OAM SYSTEM

3.1 Transmitter

3.1.1 Design on VHDL environment

To create the VHDL program of the M-OAM Modulation, the concept of BPSK (Binary Phase Shift Keying) modulation is operated.

Look Up Table named Lut Table is used to present the MGF pulses, it consists of 4 points (see Figure 5). Each one composed of 16 samples, generated by MATLAB. The max value of the pulse is "1111111111111111", the middle value is "0111111111111111", and the min value is "0000000000000000".

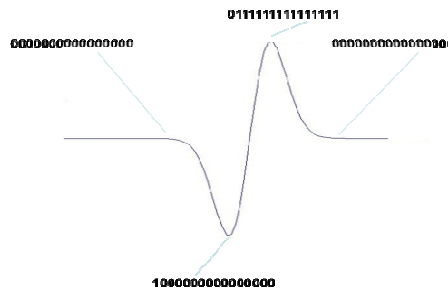


Figure 5. The used MGF pulse (G1)

The exact bits used in Look Up Table are:

```
Lut table1 = "0000000000000000"; "1000000000000000"; "0111111111111111";
"0000000000000000"
Lut table2 = "0000000000000000"; "0111111111111111"; "1000000000000000";
"0000000000000000"
Shift Pulse = "0000000000000000"; "0000000000000000"; "0000000000000000";
"0000000000000000"
```

Lut table1 and Lut table2 present the G1 pulse and its inverse respectively. To develop the 4-OAM modulation on VHDL environment, the system must read and modulate each 2 bits of the stream. The algorithm of the 4-OAM modulation is given in Figure 6.

The system modulates input data, using Look Up Table added to Shift Pulse to shape one symbol. For example if the input data is 00, the output of the system is then Lut Table1 added to Shift Pulse.

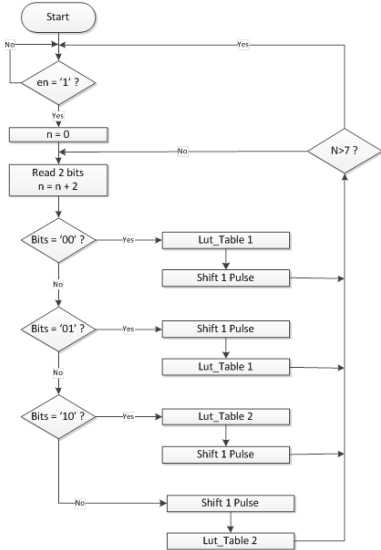


Figure 6. The VHDL development algorithm of the 4-QAM modulation

3.1.2 Simulation results

The simulations are performed using ISE Project ver.14.6 and ISim ver.14.6. In simulations, one example of the input data is "01010011". According to the modulation 4-OAM, the system should create four symbols.

The simulation result is given in Figure7. The variable p out is the result of the simulation, in other words p out is the UWB signal modulated in 4-OAM which will be transmitted. There are four symbols in the output signal.

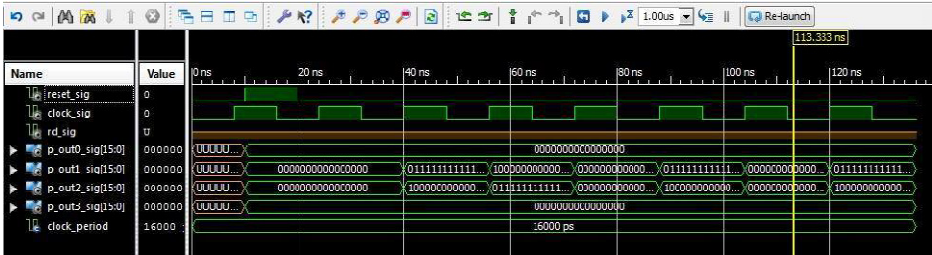


Figure 7. The simulation results of our UWB-OAM system

Each symbol consists of 8 points: 4 in the Look Up Table and 4 in the Shift Pulse. Every transmitted bit or point needs 1 clock cycle. Then, to shape one complete symbol, 8 clock cycles are used.

2.2 Receiver

2.2.1 Design of the ULTRA WIDE BAND receiver

This section explains clearly the UWB receiver components. The receiver is made of an Analog to Digital Converter (ADC), parallel correlator, peak detection and decoder as illustrated in figure 8.

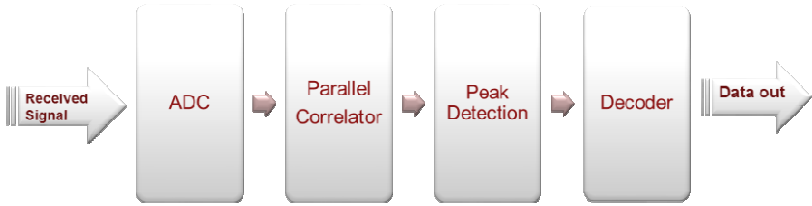


Figure 8. The block diagram of the UWB receiver

The ADC receives one symbol data of UWB train pulse at every FPGA clock. This symbol contains 16 samples and is fed to the parallel correlator to be correlated with the reference data. The maximum peak is yielded when the symbol is matched to the reference. The peak detector will detect this peak, which will be decoded by the decoder.

i. PARALLEL CORRELATOR

The ISERDES captures the data in double data rate (DDR) at the frequency clock of 375 MHz. Then, the ISERDES outputs the 4 DDR bits captured across two cycles of 1875 MHz clock. A total of 32 ISERDESs means that 128 bits (16 bytes) of data are captured in parallel at 1875 MHz, equal to 3Gbytes=second [16].

These 16 bytes can then be used to perform correlation and decoding, which needs to be pipelined since it needs to operate at the same clock speed as for the incoming data from the ADC. The results of the decoder are then passed back via a FIFO to the host application and can be read as valid received data. In this case, it is impossible to use the serial correlator. Since the data is coming in parallel, the serial correlator will cause a loss of 15 bytes data. Figure 9 shows the implemented parallel correlator block diagram.

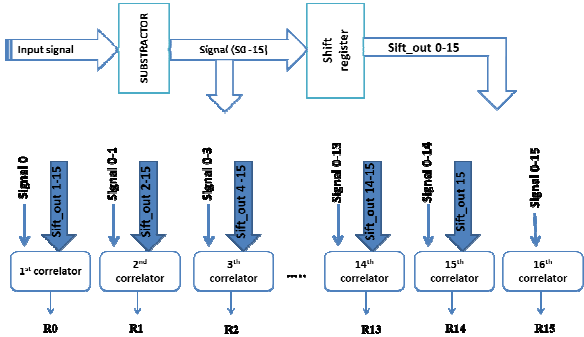


Figure 9. The parallel correlator pattern

Figure 10 describes the correlator principle. The ADC captures 16 samples in every FPGA clock. These 16 samples are then fed into the correlator block and yield 16 results of correlator at every FPGA clock.

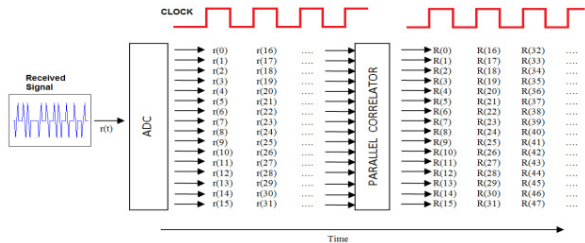


Figure 10. The parallel correlation process

For performing the 16 parallel correlations, 16 sub-correlators are created. Every sub correlator contains multiplier and adder. The multiplier is needed to multiply the input data by the reference data, and adder is used to sum the results of the multiplier. The basic principle of sub-correlator is illustrated in figure 11.

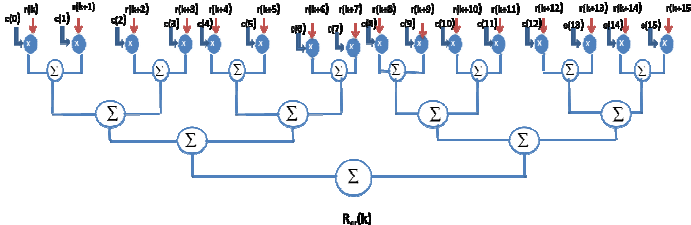


Figure 11. The principle of the sub-correlator

ii. DETECTOR BLOCK

The peak detector block is the component required to detect the peak of the correlation results. Every received symbol will be correlated with the reference symbol. If the symbol is matched to the reference, it will result a maximum peak. A threshold value is required to distinguish the signal from the noise.

a. Comparator :

To perform this separation between useful signal and the noise, a comparator block is developed. While the 16 samples are in parallel, the parallel comparator is necessary. It compares two values at every FPGA clock cycle in parallel, as illustrated in figure12.

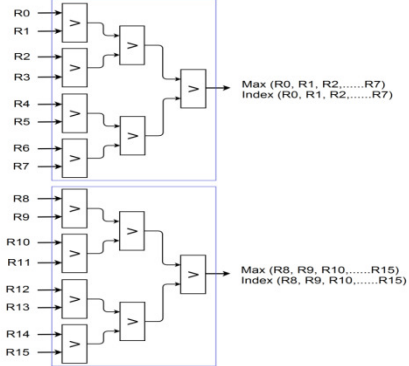


Figure 12. The comparator block

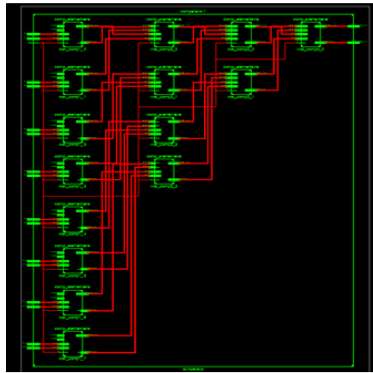


Figure 13. An RTL view of the comparator

Every transmitted symbol has the same duration of the reference. For one symbol, the UWB impulse occupies half the symbol period. It can be at the beginning of the symbol or at the end. The correlation result of every symbol will have one peak, two peaks or none. This peak can be easily detected by splitting the comparator block into two blocks: 8-higher and 8-lower block. The 8-higher block compares R8 to R15 and the 8-lower block compares R0 to R7. The comparison is performed in parallel as described in figure 11.

Figure 13 shows the implementation of the block comparator in FPGA board. The comparator results give the maximum values (peak values), index of the peak and its sign (H and L). The index is the position of the peak and the sign is the condition whether the peak exists or not. If it exists, the sign is set to 1 if not is 0. Figure 14 illustrates the representation of the existing peaks.

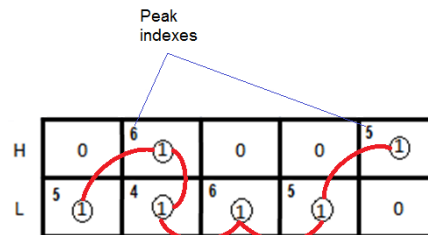


Figure 14. The representation of the peaks

iii. DECODER

Decoder block is the final process in UWB receiver system. There are two steps to decode the data: synchronization and decision.

a. Synchronization

The first step of decoder part is to synchronize the received signal. In our work, synchronization technique is based on detecting the distance between two successive peaks. As already explained above, the received signal is firstly correlated by the reference which is stored in the FPGA memory. The correlation results are then compared to find the maximum value. When it is found, it is compared to the threshold value to detect the peak. If this value is greater than the threshold, the peak is found and the H or L will be set to 1. If not, there is no peak detected and H or L is set to 0. When the first peak is detected, we start to calculate his distance to the next peak. There are

only three possibilities of such a distance: maximum, medium and minimum as described in the figure 15.

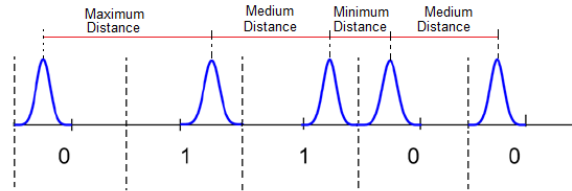


Figure 15. The distance possibilities between two successive peaks

If the distance between the two successive peaks is maximum or minimum, meaning that the symbol is started in the middle of this distance. However, for the medium distance there are two possibilities for the beginning of the symbol. Thus, there is an ambiguity. Consequently, this case cannot be used to synchronize the received signal.

b. Decision

Whenever the peak is detected, its value and index of its position are stored in FPGA memory. When the synchronization is done, these values are taken back to be decoded into data bits. To decode these data, we used the relation between the position and the polarity of the peaks. Firstly, we investigate the position of the peak to find the LSB (a least significant bit). This position is determined by the value of HL variable. If $HL = 0100$, means that the position is at the beginning of the symbol, and if $HL = 0010$ the position is at the end of the symbol. For the first case ($HL = 0100$), the LSB is 0 otherwise it is 1. Then, MSB is determined by the polarity of the peak. If the polarity is positive, means that the MSB is 0, otherwise, it is 1.

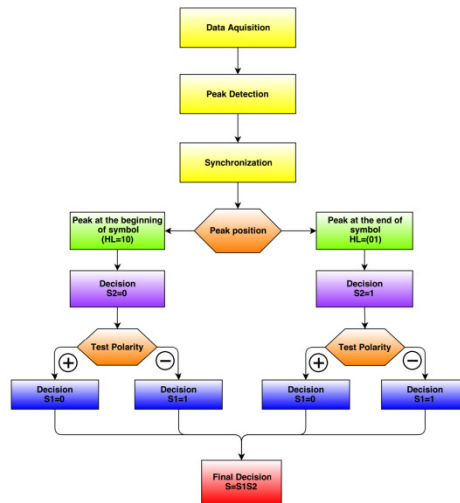


Figure 16. The decoding diagram

Flowchart of this algorithm is illustrated in the figure 16.

To conclude, the decoding algorithm can be written as follow:

Synchronization part

1. Detect the peak position.
2. Calculate the distance between two successive peaks.
3. Compare the distance with the length of the symbol. If the distance is longer than the length of the symbol, the distance is maximum. If not, re-calculate the next two peaks successive distance and go to step 3.

Decision part

4. When the maximum is found, take the middle position of the distance. This means that the symbol is started from this position. Then, return to the first symbol every 16 index position (one symbol is 16 samples).
5. When the first position is found, Investigate position and polarity of the peaks. If the position is at the beginning of the symbol, the LSB (S2) is 0 otherwise is 1. If the polarity is positive the MSB (S1) is 0, otherwise is 1.
6. Go to step 1.

2.2.2 Simulation results

The figure 17 illustrates the results of the parallel correlation. We can see that there are 16 parallel correlations on every FPGA clock cycle.

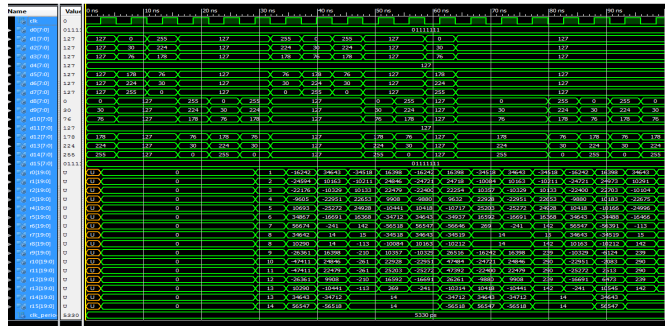


Figure 17. The simulation of the parallel correlator

The result of this simulation can be transformed into a .txt file and can be plotted by Matlab. Figure 18 is a comparison of plot correlation results between Matlab and FPGA simulation. It seems that there is almost the same result. The obtained results prove the validity of our system design in FPGA board.

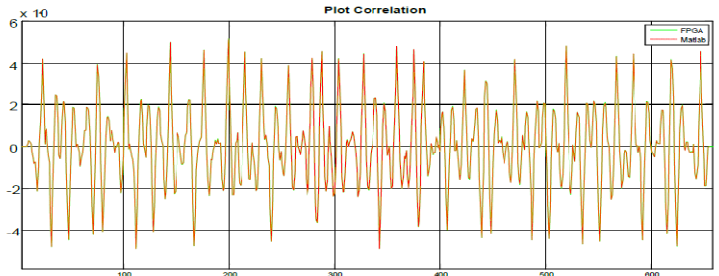


Figure 18. Comparison of correlation results by Matlab and Xilinx ISE

The figure 19 shows the simulation of the UWB receiver using ISIM Xilinx tools.

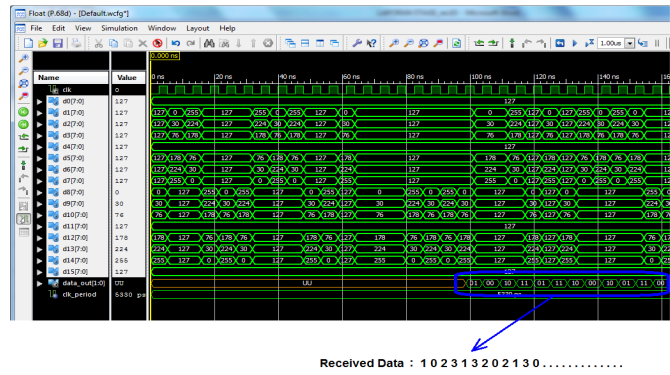


Figure 19. The decoder simulation

In this simulation, it is shown that the data are well decoded. The data is decoded into series of two bits which represent the transmitted data.

4. IMPLEMENTATION ON THE BOARDS

4.1 Transmitter

4.1.1 VHDL Programming

The four parallel data samples are required in each DAC channel because the FPGA runs at one quarter of the DAC clock speed. Indeed, the DAC is fed with 4x16-bit samples on each data clock cycle.

The FPGA uses 20s complement for the DAC values; +1V as positive full-scale, 0V , and \square 1V as negative full-scale. To shape the right pulse, we will use the max value= + 1V = 0111111111111111; middle value=0V = 0000000000000000; min value= \square 1V = 1000000000000000:

We apply this to the new Look Up Table as follows:
 Lut table1 = "0000000000000000"; "1000000000000000";
 "0111111111111111"; "0000000000000000"
 Lut table2 = "0000000000000000"; "0111111111111111";
 "1000000000000000"; "0000000000000000"

On the XRM-DAC-D4/1G, the system transmit 4x16 bits sample in 1 clock cycle. Then, to shape one complete symbol only 2 clock cycles are needed.

One of the efficient ways to achieve our objective is to adapt the UWB-OAM modulation program with the DAC Program of manufacturer. The existing ramp signal ramp data sig is then replaced by our UWB-OAM signal.

4.1.2 Transmitter Implementation Results

In order to get the right shape of the pulse signal 4-OAM, we need to understand how it works the sequencing of transmitted data. This affects the order of Look Up Table and Shift Pulse. Indeed, the order of Lut Table and Shif Pulse in asimulation is different with the one in implementation.

The order is inverted, but suitable for each purpose. For example: in simulation, to shape pulse signal of bits 00, the first bits to be transmitted is Lut Table1 and after wards Shift Pulse. However, in the implementation, the first bit to be transmitted is Shift Pulse and afterwards Lut Table1. Several combinations of bit data input are tested: 8 bit, 16 bit, 24 bit and 32 bit.

Transmitted data : 01 10 11 00

Process sequence : 00 11 01 10

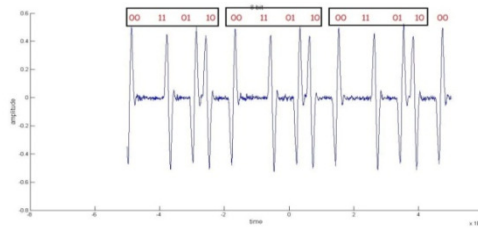


Figure 20. The transmitted signal

Transmitted data: 11 00 01 10 11 00 01 01

Process sequence : 01 10 00 11 01 10 00 11

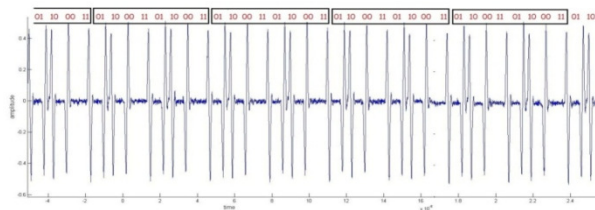


Figure 21. The transmitted signal

4.2 Receiver

The transmitted signal duration is 5.33 ns for every symbol where half of the symbol is the UWB impulse and the rest set to zero. This duration is adapted to capability of the ADC. As discussed in the previous section, the maximum ADC speed rate is 3GS/s. This means that ADC can capture 16 samples (8 bits per sample) at every FPGA clock cycle. Since one symbol is composed of 16 samples, the duration is 16/3G, equal to 5.33 ns. The used UWB impulse is Gegenbauer G1. The duration of the UWB impulse is half of the symbol, namely 2:665 ns.

4.2.1 User Interface

Figure 22 shows the developed user interface menu for UWB application using the Visual C++.

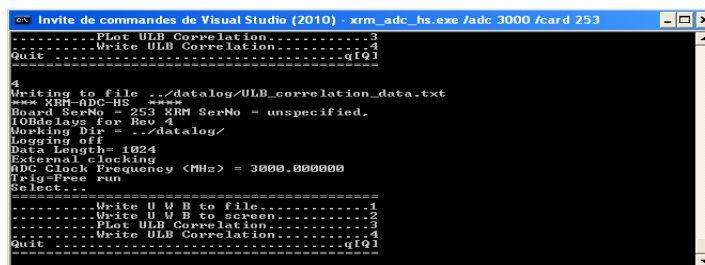


Figure 22. The developed user interface

There are four menus to investigate the results of the developed system:

1. Write UWB to file: write the captured data to file in format .txt.
2. Write UWB to screen: show directly the captured data in the screen menu.
3. Plot UWB Correlation: plot the correlated data.
- 4.

Write UWB Correlation: write the correlated data to file in format .txt.

3.2.2 Receiver Implementation Results

The test of the OAM-UWB system is performed in a laboratory conditions. Data acquisition test, UWB correlation and UWB decoder are illustrated below.

Figure 23 shows the plot of the UWB captured signal by ADC. This data can then be stored to the .txt file by choosing the Menu 1 in the application interface.

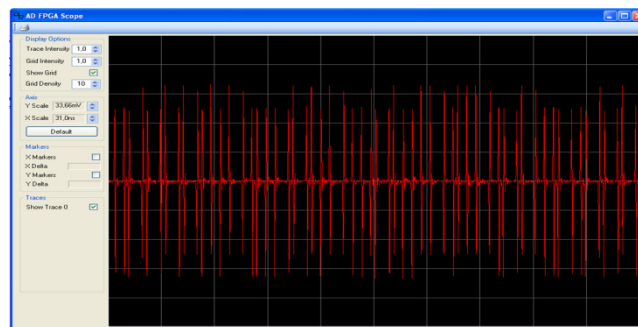


Figure 23. The UWB signal captured by the CAN

The UWB captured signal is correlated in parallel.

This correlation data is then passed to the host and can be read as in figure 24.

Figure 25 shows the result of the decoded data. The series of data 2 3 2 1 0 1 0 3 2 0 2 1 3 1 2 1 2 0 0 3 were sent.

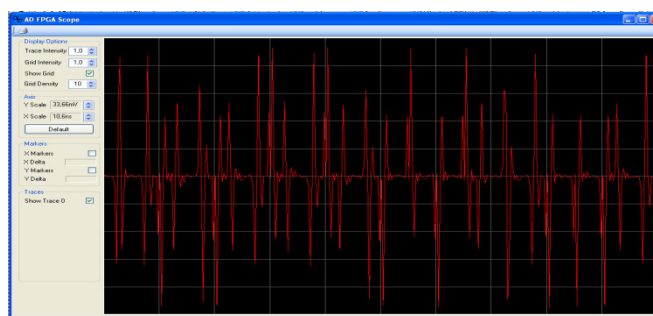


Figure 24. The correlation result

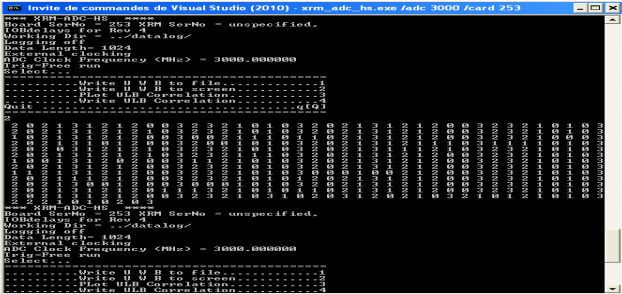


Figure 25. The result of the decoded data

From figure 25, it seems that the received signal is decoded well to recover the transmitted data. Thus, the performances of our system implementation give remarkable results and validate the simulation work.

5. CONCLUSION

The main objective of this paper is to implement an Ultra - wideband (UWB) communication system using the new modulation technique M-OAM (Orthogonal Amplitude Modulation) on the FPGA board. This work is divided into two parts, simulation and implementation. The simulation step involves VHDL programming for UWB system with 4-OAM modulation and ISIM software. While, the implementation part requires VHDL program used in the simulation. Converters ADC and DAC with their programs provided by the manufacturer, FPGA card, and an oscilloscope are used. VHDL program from the simulation cannot be used directly in the implementation process. It should be modified to satisfy the requirement of the converters card.

Thus, the DAC program from the manufacturer is modified to accommodate the new UWB-OAM program. The system has been tested using both the FPGA and the converters platforms under laboratory conditions. The ADC has been performed to capture UWB signal.

To read the data captured by the ADC, an interface from the ADC data to the PC was successfully developed using visual C++. Results show that the implemented system was able to capture UWB signal and decode it back to the valid data. For further study, it is an interesting challenge to develop a same communication system based on FPGA for high order modulations such as 16-OAM and 64-OAM.

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