Solder fatigue failures in a new designed power module under Power Cycling

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ABSTRACT

Today a point has been reached where lifetimes of power modules are limited by the standard packaging technologies, such as wire bonding. To surpass these limits, a new power module was designed using Cu clips as interconnects instead of Al wire bonds. With this new design the structure robustness should be improved and lead to a reliability gain but in counterpart it requires an additional solder layer in order to fix the clip onto the die. This paper studies the failure mechanisms occurring in these two solder layers under power cycling. The behavior of solder layers is precisely analyzed by performing power cycling tests and by taking advantage of Finite Elements simulations. Furthermore an experimental and numerical sensitivity study on test parameters is conducted. Results obtained enable the definition of solder lifetime prediction models.

1. Introduction

To improve the reliability of power devices, a power module with a new architecture has been developed. This module is molded and does not have Al wire bonds but a copper clip as interconnect. It results in a more complicated internal structure than in standard modules. Indeed, the use of a Cu clip implies an additional solder layer in order to fix the clip onto the die. Solder fatigue failures occurring in such a power module with a chip soldered on its both sides were not studied in the literature yet. But solder joints long term reliability is an ultimate requirement for electronics packaging. Indeed, solder joints serve 3 important purposes: they are an electrical inter-connect, a mechanical bond, and must often serve as a thermal conduit to remove heat from joined devices. Focusing specifically on the mechanical wear out mechanism, most fatigue failures can be attributed to thermomechanical stresses in the soldered joints, caused by differences in the Coefficient of Thermal Expansion (CTE). Most components are mounted on substrates that can expand and contract at rates different from that of the components. This CTE mismatch can strain solder joint connections, and over the component lifetime can contribute to mechanical solder joint fatigue failure [1]. Actually solder joint failure occurs in very complex mechanisms probably involving the interaction of several basic failure processes, and among them, the creep phenomenon. Creep is defined as a time-dependent deformation occurring when a material is subjected to a stress for a prolonged period of time and under high temperature in relation to the melting point of the material [2].

Early solder joint fatigue models were developed mostly for Ball Grid Array (BGA) packages with leaded [1] and later lead-free solder [3,4] under thermal cycling conditions. It is interesting to notice that in [3,4], thanks to the help of Finite Element Analysis (FEA), both accumulated creep strain and creep strain energy density based models were developed.

Then, in recent year, several papers related to power cycling have been published. But, many of them are still comparing the fatigue life model of lead BGA packages under thermal and under power cycling [5–8]. Popps et al [7] did an experimental study, Rodgers et al [8] showed a detailed FEA, and Towashiraporn et al [6] suggested predictive reliability models through empirical correlation as well as FEA. Only 3 papers comparing the fatigue life under thermal and power cycling conditions are investigating lead free solders [9–11]. Laurila et al [11] and Li et al [9] studied the evolution of microstructure and failure mechanisms respectively for a through hole power diode and for a TFBGA. Petrone et al [10] investigated a SMD with ribbons as interconnects instead of traditional Al wire bonds. Perkins [12] developed lifetime prediction models for lead solders of a Ceramic BGA subjected to combined thermal and power cycling and vibration environment. Among all those cited papers, only one manages to vary the power cycling conditions

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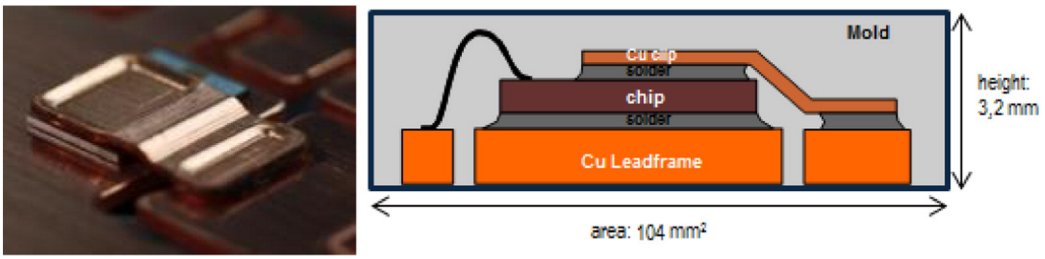


Fig. 1. On the left a picture of the MOSFET with a copper clip. On the right a schematic cross-section of one MOSFET assembly.

[5]. But none of them studied the influence of power cycling conditions on fatigue models of solder joints and none of them predict the lifetime based on the accumulated creep strain in one cycle.

In the present work, failure mechanisms occurring under power cycling in both solder layers of our new designed module are analyzed using experiments and FEA. The influence of power cycling parameters on the accumulated creep strain in one cycle is presented in a sensitivity study. The accumulated creep strain is then defined as a damage parameter, allowing the determination of fatigue models for both solder joints.

2. Design of power modules

The power module used in this study is a package made of 6 newly designed Metal Oxide Semiconductor Field Effect Transistors (MOSFET). Indeed, those MOSFETs have an electric connection achieved by a copper clip soldered on top of the chip instead of using wire bond (Fig. 1). The chip and MOSFET assembly dimensions are the following:

- Chip: length: 4.5 mm, width: 3.12 mm, height: 0.175 mm and area: 14 mm^2
- MOSFET assembly: length: 13 mm, width: 8 mm, height: 3.2 mm, and area: 104 mm^2

This structure is expected to be more reliable because it avoids wire bond fatigue failures, often the root cause for the device failure. The inner structure of this MOSFET is a bit more complicated than the one of standard power modules. It has some additional material layers on top of the others between the chip and the copper clip (Fig. 2).

3. Experimental and numerical methods

3.1. Experiments

Active Power Cycling (APC) is the most important reliability test for power modules as it reproduces real working conditions. The device under test is mounted onto a liquid-cooled heat sink and only one MOSFET of the package is electrically loaded. Usually the load current is conducted by the power chip and the power losses heat up the package. Here, the heating current has opposite polarity and is conducted by the body diode of the MOSFET. When the maximum target temperature within the diode is reached, the load current is switched off and the system cools down to a minimum temperature. The end of the cycle is achieved when the minimal temperature is reached. The next cycle begins by starting the load current again.

About 30 samples were tested varying the minimum junction temperature T_{jmin}, the temperature swing ΔT_j and the power on-time t_{on} (also called pulse width). The test strategy used here consists in adjusting the loading current to the desired temperature swing ΔT_j and then to repeat the cycle with constant pulse width t_{on}. The temperature swing is defined at the start, but may vary with ageing effects of the device. This strategy is the most severe method but the closest one to application.

During APC, the forward voltage V_f of the body diode and the junction's temperature swing ΔT_j are monitored as they are good indicators of modules health. Indeed, both parameters are likely to increase with ageing effects. T_j is measured via V_f which is a Thermo-Sensitive Parameter (TSP). The thermal impedance Z_{th} was not measured during APC test, but was deduced from V_f and ΔT_j which are time dependent, using the formula:

$$Z_{th}(t) = \frac{\Delta T_j(t)}{Pv} = \frac{\Delta T_j(t)}{I \; V_f(t)} \tag{1}$$

Where P_v is the power, t the time and I is a constant current.

Before starting the test and at the end of it, power modules are electrically and thermally characterized by measuring leak currents, the drain to source on state resistance R_{DSon} and the thermal impedance Z_{th}. The goal is to evaluate the healthiness of modules after cycling. Metallographic analyses were carried out on tested modules in order to investigate the defects.

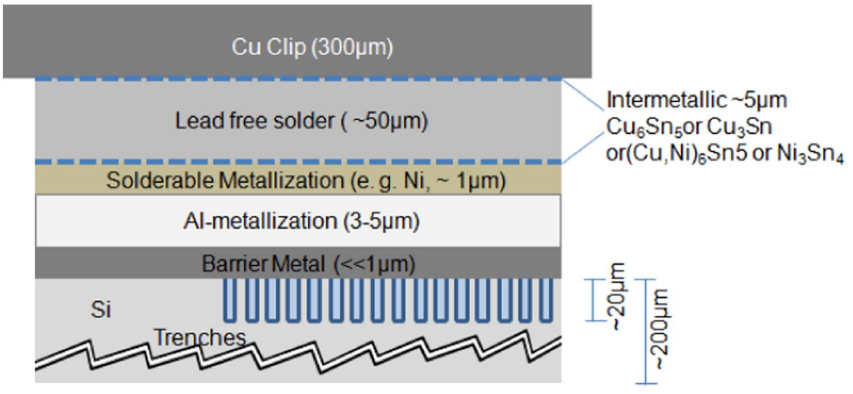


Fig. 2. Detail of the layer structure between the chip and the Cu clip.

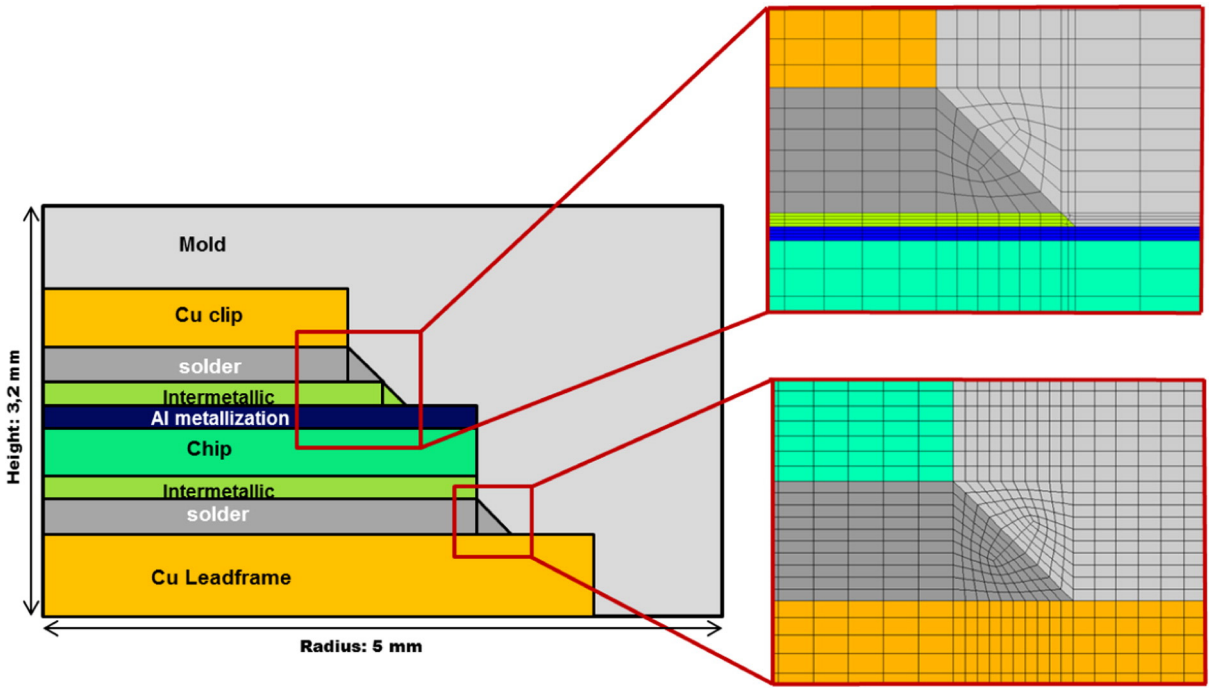


Fig. 3. Schematic 2D section of the power device used for simulation with a focus on the mesh at both solders meniscus.

3.2. Simulations

A 2D FE model has been created for a MOSFET with an axisymmetry condition (Fig. 3). Such a simplified model of the power package is possible because MOSFETs included in the package are thermally decoupled, meaning that every MOSFET acts as a single one. Moreover, this 2D axisymmetric model with chip-midpoint as symmetry axis is suitable to represent the physical phenomena occurring in the MOSFET, as the electrical current flows through the center of the chip. Thus the chip-midpoint corresponds to the neutral point in terms of thermal expansion. So, in our case plane stress or plane strain approximations would not have been a wise choice. Additionally the results obtained with the 2D axisymmetrical model were compared to the ones obtained from a full 3D model of the MOSFET. Results were found to be similar in both simulations, thus it was proven that the 2D axisymmetrical model provided reliable and precise results.

In this FE model, a fine mesh is defined using quadratic plane elements with 8 nodes. The thinnest layers have a minimum of 4 elements in their thickness, which means that the smallest elements have a size of about 1 μm. Attention was also paid to refine the mesh in the most critical areas of the module (Fig. 3). Both solder layers have fine elements with an aspect ratio of 2.8 and critical areas of the metallization and the intermetallic layer have elements with an aspect ratio of 6.5, which guarantee reliable results. Some elements have a bigger aspect ratio, up to 35, but these elements are not located in critical areas and thus did neither affect the convergence nor results.

Thermo-mechanical analysis is performed, which means that thermal results of the transient thermal simulation are imported as loads in the thermo-mechanical simulation. In the thermal analysis, the module is mounted onto a heat sink of aluminum with a constant temperature assumed at its bottom line. Free convection and radiation coming from the air are also taking place on the exterior surfaces of the module. During APC, the chip generates heat which is then dissipated in the entire module. In the mechanical analysis, the power module is not subjected to any pure mechanical loads, the module is only fixed at one point and loads are thermally induced. Three cycles are simulated after an initial cooling down from the stress free temperature of the module to the ambient temperature.

The elasto-plastic properties of the copper of the lead frame and the clip were characterized and modeled by a bilinear kinematic hardening.

As the study focusses on solder degradation, it is therefore important to accurately model the thermo-mechanical behavior of the solder (Table 1).

The SAC solder alloy behavior was characterized by [3] using a Garofalo model which defines the secondary creep rate as a function of stress and temperature with a hyperbolic sine, as follow:

$$\dot{\varepsilon}_{cr} = C_1[sinh(C_2 \quad \sigma)^{C_3} e^{C_4/T} \tag{2}$$

Where $\dot{\varepsilon}_{cr}$ is the steady-state creep rate, σ the stress in MPa, T the temperature in K, and C_1 through C_4 are constants defined as follow in Table 2:

Table 2
Table of values for the constants of the Garofalo creep law for the SAC solder alloy.

Constant C1 (1/s)	Constant C2 (1/MPa)	Constant C3 (-)	Constant C4 (K)
277984	0.02447	6.41	6500

Table 1
Table of thermo-mechanical properties of the SAC solder alloy.

Density (kg/m^3)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poissons ratio	CTE (ppm/K)
7300	from -73°C to 225°C	238	60	49551 - 32001	0,36	20

Table 3
Table of thermo-mechanical properties of the intermetallics(IMC).

Density (kg/m^3)	Temperature (°C)	Specific Heat (J/kgK)	Heat Conductivity (W/mK)	Young's Modulus (MPa)	Poissons ratio	CTE (ppm/K)
8280	from 25°C to 175°C	286	34,1	100000	0,309	18-20,2

Table 4
Recap chart of 13 of the 30 APC tests performed with the resulting bottom solder degradations.

T_{jmin}	-30° C				15°C					45°C ≤ Tjmin ≤ 70°C				
ΔT_j	60K	120 K			60 K	90 K	120K			60K	90 K			110K
t_{on}	0,2s	0,5s	2s	5s	0,2s	0,5s	0,5s	2s	7s	0,2s	0,2s	2s		0,35s
t_{off}	0,8s	2,5s	7s	10s	3s	4,5s	3,5s	6s	5s	1,2s	2,8s	5s		1,15s
Number of cycles	3 000 000	510 000	110 000	220 000	1 000 000	830 000	1 430 000	911 000	61 640	2 270 000	2 068 510	900 702		629 543
increase in Vf	-	+ 3,5%	+ 1%	+ 6%	-	+ 0,5%	+ 6,5%	problem	+ 1%	+ 1%	-	-		+ 6,6%
increase in ΔT	-	+ 17%	+ 3,5%	+ 12,5%	-	-	+ 8,3%	problem	0	-	-	-		+ 22%
increase in Z_{th} at 0,01s	+ 2,75%	-	+ 16%	+ 36,5%	-	-	+ 2%	-	-	-	-	-		yes
Degradations in bottom solder	-	cracks at chip edges	cracks at chip edges	long cracks and voids at chip edges	-	recrystallization and voids at chip edges	voids and cracks at interface with CuLF and big voids under the clip	strong recrystallization and cracks at chip edges and cracks at interface with CuLF	cracks at chip edges	-	cracks at chip edges	cracks at chip edges and at the interface with CuLF		cracks and thick IMC layer at chip edges
% degraded surface	-	-	35	66,67	-	-	42,4	4	40	-	15,2	8,8		-

Fig. 4. Example of a slight increase in Z_{th} after 110 000 APC cycles with T_{jmin} = -30°C, ΔT_j = 120K, t_{on} = 2s.

The bond between the soldered partners is mainly provided by the formation of one or more intermetallic (IMC) phases. In the case of a SAC solder, two copper rich IMC are formed: Cu_6Sn_5 and to a smaller extend Cu_3Sn. Here, one layer of IMC is modelled between the Al metallization and the top solder, and is assumed to be pure Cu_6Sn_5. Its material properties (Table 3) were defined based on literature's data [13,14], and as IMC are brittle materials, a linear elastic model was employed.

The brittle silicon of the chip has linear elastic properties. The chip-metallization is made with an AlCu alloy containing 0.1 % up to 1% Cu. Its material model uses a bilinear kinematic hardening to describe the elasto-plastic behavior of the metallization [15].

The commercially available epoxy-based molding compound is a polymer, and has thus a viscoelastic behavior. The material model is restricted to be thermorheologically simple. Its master curve was implemented through the use of Prony series and the shift operation was defined with the Williams-Landel-Ferry (WLF) shift function. During the assembly process, just after the encapsulation, a post mold cure process takes place. It consists in exposing the module to elevated temperatures, in general 175°C, to speed up the curing process and expedites the cross-linking process of the polymer's molecules. Thus in order to take into account residual stresses due to post mold cure, the stress-free temperature of mold is assumed to be higher (195°C), than the one of the other materials (175°C).

With the thermo-mechanical simulation, evolutions of stresses and creep strains in both solder layers are monitored during power pulses. A study of the sensitivity of various test parameters (minimum junction temperature T_{jmin}, temperature swing ΔT_j, and pulse width t_{on}) is also simulated and the influence of those parameters on the mechanical behavior of solder layers is quantified.

4. Degradations observed in solders and intermetallics after power cycling tests

Some APC tests were performed on MOSFETs with different experimental parameters: T_{jmin} ranges from -30°C to 60°C, ΔT_j varies from 60K to 120K and t_{on} ranges from 0.2s to 10s. Tests were stopped arbitrarily when an important increase in the monitored body diode forward voltage V_f or temperature swing ΔT_j was noticed. There was no fixed end-of-life criterion defined as this one still has to be determined for this kind of module. Tests were stopped usually after 100.000 to 2 million cycles, and modules were always electrically functional at the end of tests. This proves the high reliability of such power modules with double sided soldered chips. Despite this very good endurance, modules are submitted to degradation phenomena, and both solder layers are affected by thermally induced fatigue.

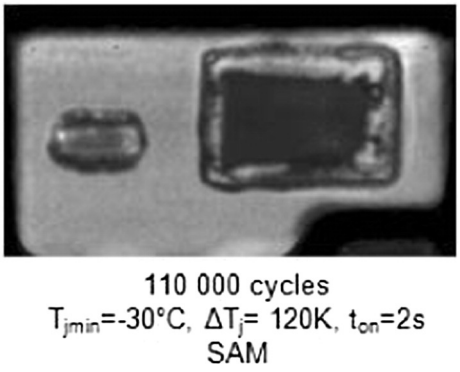


Fig. 5. SAM image of a bottom solder with degraded edges.

4.1. Degradations in the bottom solder

About 30 tests with different parameters were performed and analyzed, but for sake of clarity only 13 of them are taken as representative examples for bottom solder degradations and are shown in the Table 4. When a sign "–"appears in the table, it means that there was no increase in parameter or no degradations observed.

An increase in the Z_{th} measurement can indicate the presence of damages in the bottom solder (Fig. 4). Indeed, the main thermal path is at the bottom of the package: the heat flows from the chip through the bottom solder and the Cu lead frame to the heat sink. So, when the bottom solder is degraded, it affects the thermal path, thus the thermal impedance Z_{th} slightly increases at about 0.001s and until the end of the measurement (10s). In our case the maximum of Z_{th} increase seems to be reached at 0.01s.

In order to confirm the suspicion of damages in the bottom solder, modules are first scanned by a Scanning Acoustic Microscope (SAM). Then, metallographic specimens of tested devices were prepared and defects investigated into using Optical Microscope (OM) and Reflection Electron Microscope (REM). Thanks to the SAM, we can observe that solder degradations are typically occurring at the edges (Fig. 5). For some cases it was even possible to measure the white area visible at the edges of the SAM pictures. This gives us a measure of the degraded surface which constitute a quantitative idea on the importance of bottom solder's degradations.

Then the observation of metallographic specimens with OM and REM confirms that solder degradations are occurring at chip edges and gives us more details about this phenomenon. First different types of solder degradations were observed (Fig. 6): recrystallization, voids and cracks as well as an increase in the thickness of IMCs. The fact that recrystallization, voids and cracks all occurred at chip edges shows that chip edges solder's areas are critical regions of strain concentration where microstructural changes are initiated and propagate with APC. Actually, here, microstructural changes seem to occur in the 4 different phases of recovery, recrystallization, intergranular cracking and coalescence of cracks, described by Mattila et al. [16]. With the pictures Fig. 6, we can remark that first the recrystallization occurs at chip edges and propagate toward chip center. Then, voids appear in the area subjected to recrystallization, and these voids coalesce to form a crack. This solder crack starts underneath the chip edge, propagates in a round shape to the bulk solder and finally propagates straight toward the center of the chip. Sometimes it was also noticed that cracks located at chip edges were propagating close to the interface with the IMC layer. Cracks propagating from chip edges toward chip center were also described in the literature for standard modules with Al wire bonds and lead free die attach [17,18]. And the paper [19] also reported cracks formation

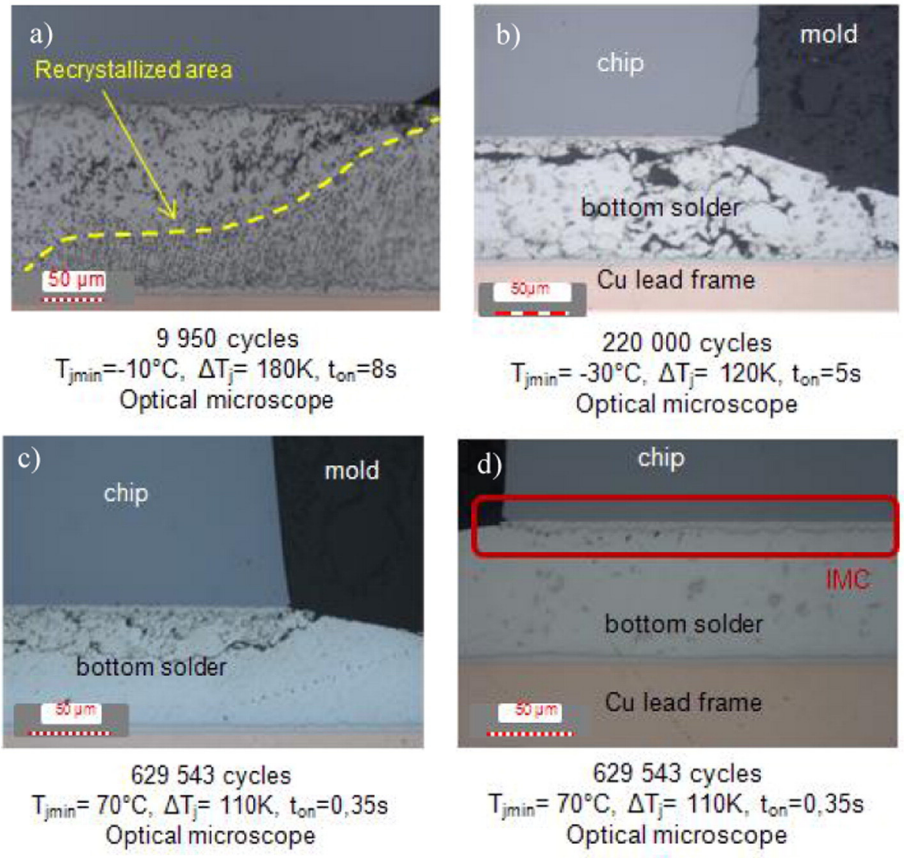


Table 5
Recap chart of 12 of the 30 APC tests performed and the resulting top solder degradations.

T_{jmin}	-30 °C				15°C				60°C ≤ Tjmin ≤ 70°C			
ΔT_j	60K	120 K			60 K	90 K	120 K		60K	80K		11 OK
t_{on}	0,2s	0,5s	2s	5s	0,2s	0,5s	0,2s	0,5s	0,2s	0,5s		0,35s
t_{off}	0,8s	2,5s	7s	10s	3s	4,5s	3,8s	3,5s	1,2s	1s		1,15s
Number of cycles	3 000 000	510 000	110 000	220 000	1 000 000	830 000	800 000	1 000 000	2 270 000	1 380 000		629 543
increase in Vf	-	+3,5%	+1%	+6%	-	+0,5%	+10,75%	+4%	+1%	-		+5,6%
increase in ΔT	-	+17%	+3,5%	+12,5%	-	-	+5%	+4%	-	-		+22%
Degradation in top solder	-	cracks and voids at meniscus above the chip	delamination at interface with Al and cracks at meniscus	cracks at interface with Al and presence of Al and IMC at meniscus above the chip	voids at grain boundaries at meniscus and along Cu clip and recrystallization above the chip	voids at grain boundaries and recrystallization at meniscus and along Cu clip	cracks at interface with IMC above the chip at meniscus and recrystallization at cracks	cracks at meniscus above the chip, voids and cracks along Cu clip and strong recrystallization at meniscus	voids at meniscus	-	cracks and voids at interface with IMC above the chip, presence of Al and strong recrystallization at meniscus	strong degradation of almost the entire clip surface with voids and cracks above the chip, voids and presence Al at meniscus
% delaminated surface top solder/AlCu	-	44,44	50	-	-	-	81,75	85	-	-	33,33	73,33

between the IMC and the solder in the case of a lead-free solder. The phenomenon of an increase in the thickness of the IMC layer due to APC is also known and was already observed by Laurila et al. [11].

The study of the Table 4 and of the Fig. 6 allows determining the influence that some parameters can have on solder degradations. First, one can notice that for tests performed with a field load of $\Delta T_j = 60K$, no significant increase in V_f or in ΔT_j were registered even after several millions of cycles. Moreover the metallographic analysis of these samples did not reveal any degradation in the bottom solder. Whereas for $\Delta T_j = 90K$ or 120K increase in V_f or in ΔT_j were registered and metallographic specimens were showing solder degradations. This shows that increasing the ΔT_j leads to more severe degradations in the bottom solder. Actually this can also raise the question to know if the same failure mechanism occurs under $\Delta T_j = 60K$ and under $\Delta T_j = 90K$ or 120K. Concerning the influence of t_{on}, it appears that increasing t_{on} leads to more important solder degradations: voids and cracks are longer and the degraded surface is bigger with long pulses than with short pulses. This appears quite clearly for the case with $T_{jmin} = -30°C$ and $\Delta T_j = 120K$. The influence of T_{jmin} on solder degradation is difficult to determine solely with our results. Some more tests may help to have a better idea of the role played by T_{jmin} on solder failure.

4.2. Degradations in the top solder

Here again for sake of clarity, some representative cases in terms of top solder's degradations were taken out of the 30 tests performed and are presented in the Table 5.

No electrical or thermal measurements are able to give information regarding degradations in the top solder. Indeed, degradations of the top solder will only have a negligible impact on the R_{DSon} increase. Moreover, as the clip evacuates less than 5% of the heat generated by the chip, no significant increase in the Z_{th} is expected due to top solder degradations. To evaluate the integrity of the top solder, metallographic specimen of tested devices have to be prepared and defects investigated into using OM and REM. Different types of degradations occurring in the top solder were highlighted (Fig. 7): recrystallization, voids and cracks as well as delamination at the interface with Al metallization or with IMC. These degradations are taking place most of the time at the top solder meniscus, above the chip, but also at the meniscus along the Cu clip. The degradations observed are similar to the ones occurring in the bottom solder. But damages in the top solder are also influenced by the specific geometry of the Cu clip. Indeed, the top solder meniscus has to follow the round shape of the clip, and quite often voids and cracks were observed close to the Cu clip (Fig. 7c). The types of degradations and their locations occurring in the top solder cannot be compared to the literature, as only few papers studied module with clip, and when they did, the clip attach was not the focus of the study.

The study of the Table 5 allows determining the influence of some parameters on top solder degradations. First, on can notice that for the 3 tests performed with $\Delta T_j = 60K$ no significant increase in V_f or in ΔT_j were registered even after 1 to 3 million of cycles. Moreover for 2 of those tests, no degradations were observed in the top solder. For the third test with $T_{jmin} = 15°C$, degradations reported can be considered as minor as only recrystallization and voids are observed but no cracks. Whereas for $\Delta T_j = 90K$ or 120K increase in V_f or in ΔT_j were registered and metallographic specimens were showing solder degradations. So this confirms that high ΔT_j are accelerating the degradation of solder layers. And it raises again the question of different failure mechanisms occurring under different ΔT_j. Regarding t_{on}, it appears that increasing t_{on} leads to more important solder degradations: voids and cracks are longer and the degraded surface is bigger with long pulses than with short pulses. This appears quite clearly for the case with $T_{jmin} = -30°C$ and $\Delta T_j = 120K$. Finally, here also, the influence of T_{jmin} on top solder degradation is difficult to determine solely with our results.

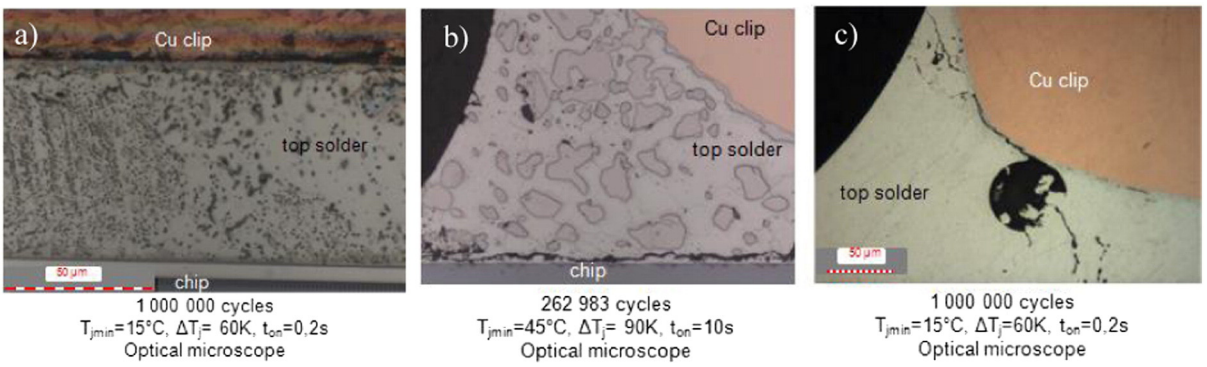


Fig. 7. a) Recrystallization, b) voids and cracks at the meniscus above the chip and c) voids and cracks at the meniscus along the Cu clip.

5. Simulation results

First, the temperature profile in the chip was studied: a path crossing the chip laterally in its middle was defined and the lateral temperature profile in the chip is plotted at the end of a heating phase with T_{jmin} = -40°C, ΔT_j = 120K, t_{on} = 10s (Fig. 8). Then, mechanical stresses and deformations were investigated. After cycling, a slight bending of the module and a shrinkage of the mold are observed [15]. Whatever the temperature, the chip is entirely submitted to in-plane compression, while the other layers are submitted to low tensile stresses. Because of the mold that compresses the whole assembly together, out-of-plane stresses are almost inexistent in the module. Shear stresses also appear to be limited in the module, except at the chip extremity at the interface with the bottom solder meniscus, where the maximum of shear stress (109 MPa) is reached (Fig. 9).

Then, we focused our study on both solder layers. As seen in experiments, solder joint failures are occurring in both bottom and top solder under APC. Solder joint failure involves complex mechanisms, and among them the creep phenomenon. Creep deformation does not occur suddenly upon the application of stress. Instead, strain accumulates as a result of long-term stress. Therefore, we investigated the accumulated creep strain as it is a good indicator of solder joints healthiness. For the bottom solder, the von Mises stress was also studied in order to better understand the mechanisms involved.

5.1. Bottom solder behavior

The creep strain in the bottom solder is analyzed via a path defined at the location where cracks are frequently occurring after cycling in standard module: at the layer extremity and at the height of 1/8 of the layer thickness underneath the chip. For our module, the creep strain analysis can also be performed at this specific height as a maximum of creep strain is to be seen in this area. The accumulated creep strain for one cycle is calculated by averaging the creep strain along a path, whose width has to be determined. After APC tests, some cracks were measured and had an average length of 10% of the total bottom solder length, with extreme cases having a length reaching up to 5% and 40%. In order to identify the influence of the path width on the creep calculus, the accumulated creep strain during 3 cycles was calculated for several different widths of path ranging from 5% to 20% of the bottom solder radius (Fig. 10). The different curves are approximately parallel to each other if we exclude the 5% radius one. This means that with a path width between 10% and 20%, no significant difference will appear in the resulting accumulated creep strain calculated by the numerical model. Thus, a radius of 10% was taken, as a crack with such a length would represent a degradation of 20% of the thermal path, which is a critical limit. The amount of accumulated creep strain per cycle for the 10% radius path, begins to be stabilized for the last cycle (3rd cycle).

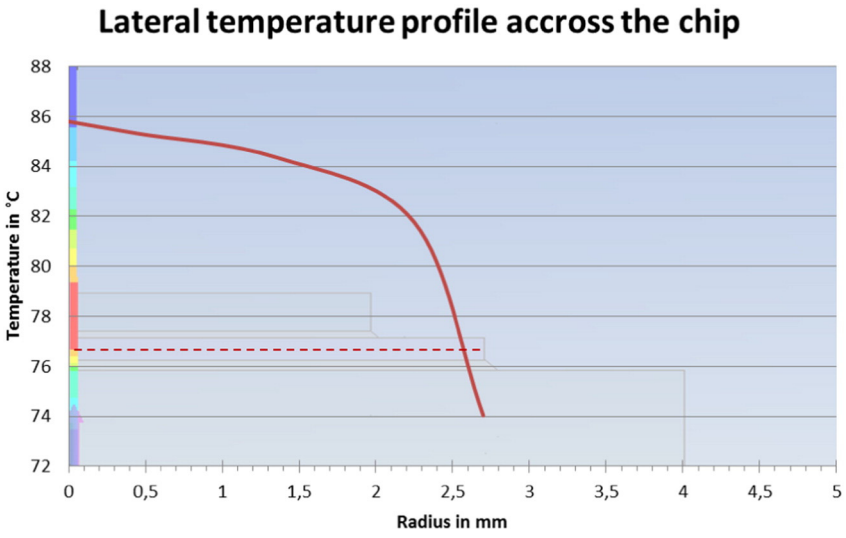


Fig. 8. Lateral temperature profile across the chip at the end of a heating phase with T_{jmin} = -40°C, ΔT_j = 120K, t_{on}

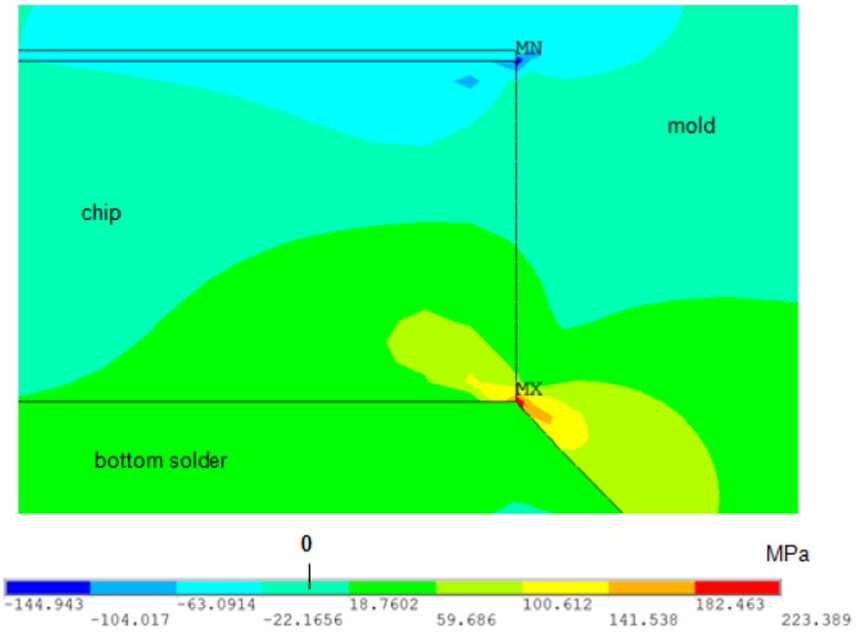
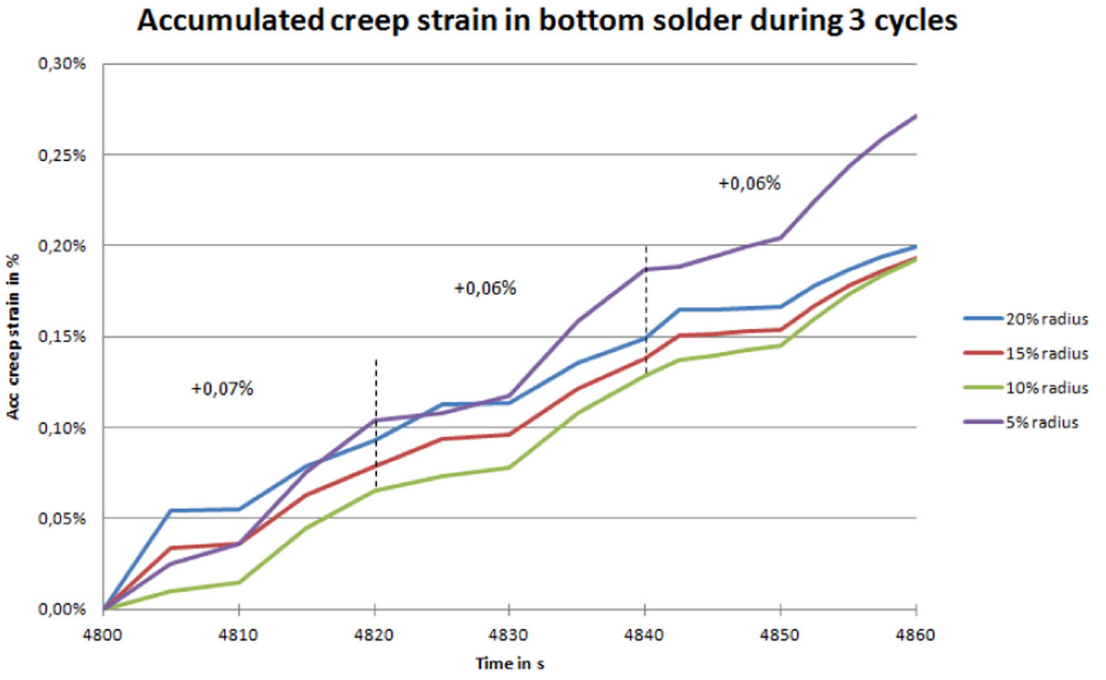


Fig. 9. Shear stress at -40°C at the interface chip/bottom solder meniscus.

The evolution of temperature, von Mises stress and accumulated creep strain in the last cycle at the critical area of the bottom solder is plotted for one case on the Fig. 11. The initial von Mises stress value is relatively high as a 175°C stress free temperature was defined and the cycle starts at -40°C. By heating up, the stress decreases and reaches a minimum value. By continuing heating up, the stress changes its direction thus the von Mises stress increases. Then the temperature stays constant, and we observe a stress relaxation. By starting the cooling phase, the stress reaches a minimum value and increases by decreasing temperature. The accumulated creep strain follows the temperature changes and starts to increase at the beginning of heating up or cooling down. At constant temperature the creep strain continues to increase. Thus the t_{on} can have a significant influence on the creep state in solder. The accumulation of creep strain is much lower for heating phase than for cooling phase. In one cycle the bottom solder accumulates 0.064 % of creep strain.

5.2. Top solder behavior

The creep strain is analyzed with the same method as for the bottom solder. Here a path is defined at 7/8 of the thickness underneath the clip, as the maximum of creep is to be seen in this region. For the top solder, it was very difficult to measure crack lengths, thus no experimental data are available, but the same study as for the bottom solder was done, concerning the path width influence on the calculated creep. Here also it was found that for a path width between



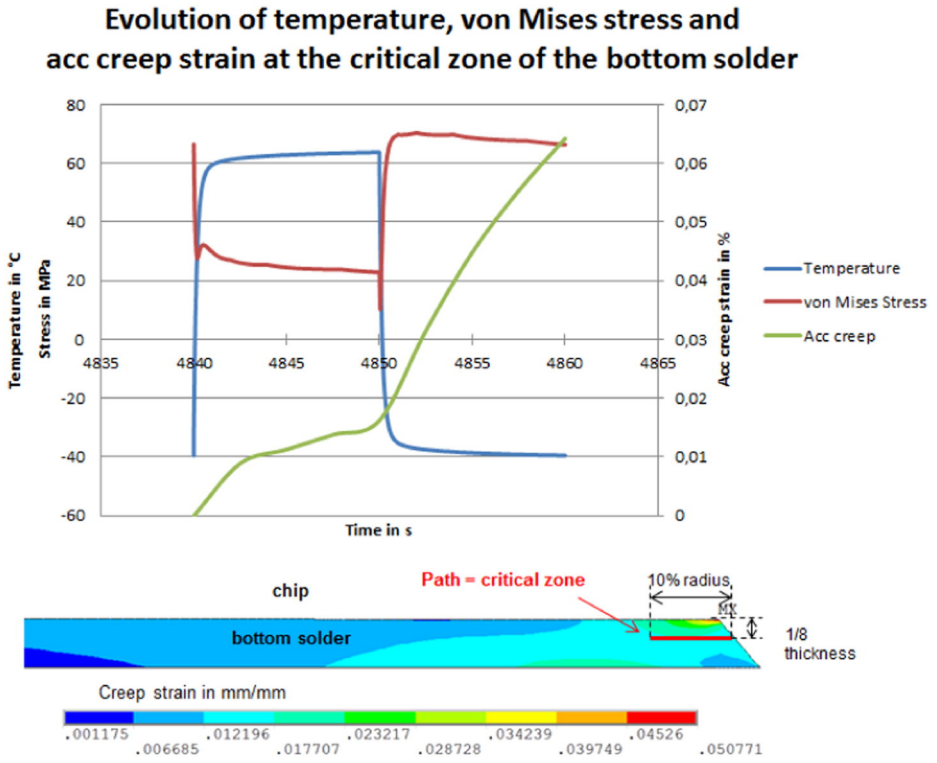


Fig. 11. Evolution of temperature, von Mises stress and accumulated creep strain at the critical zone of the bottom solder during the last cycle for the case $T_{jmin} = -40°C$, $\Delta T_j = 120K$, $t_{on} = 10s$.

10% and 20% no significant difference in accumulated creep strain appears. Thus a radius of 10% is taken by analogy with the bottom solder. The amount of accumulated creep strain per cycle begins to be stabilized for the last cycle (3rd cycle). The accumulated creep strain in the last cycle at the critical area of the top solder is plotted Fig. 12. So in one cycle the top solder reaches 0.28 % of accumulated creep strain. So the top solder accumulated a lot more creep than the bottom solder does.

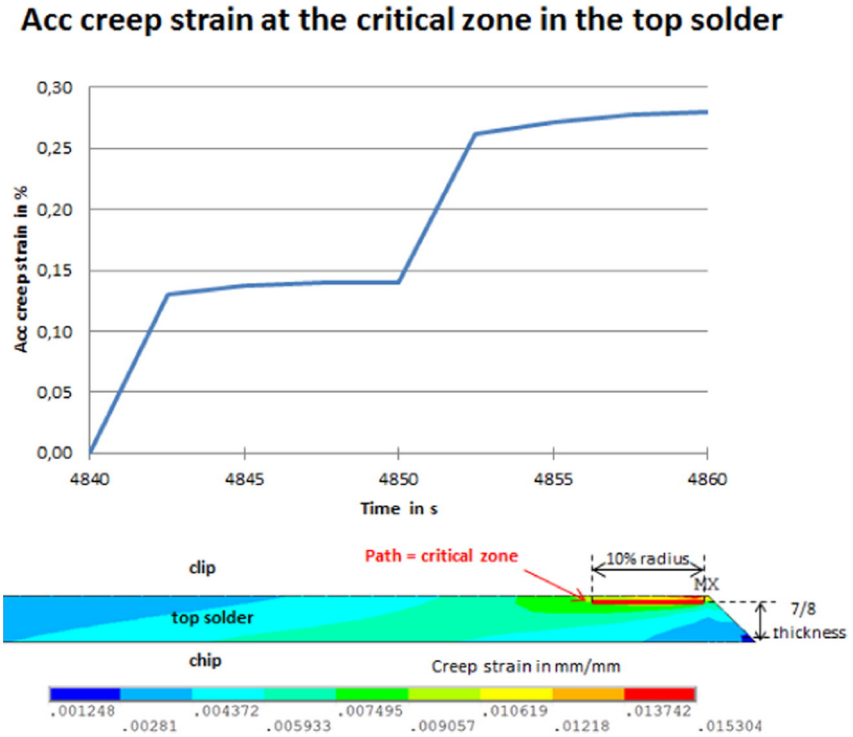


Fig. 12. Accumulated creep strain in the critical zone of the top solder during the last cycle for the case $T_{jmin} = -40°C$, $\Delta T_j = 120K$, $t_{on} = 10s$.

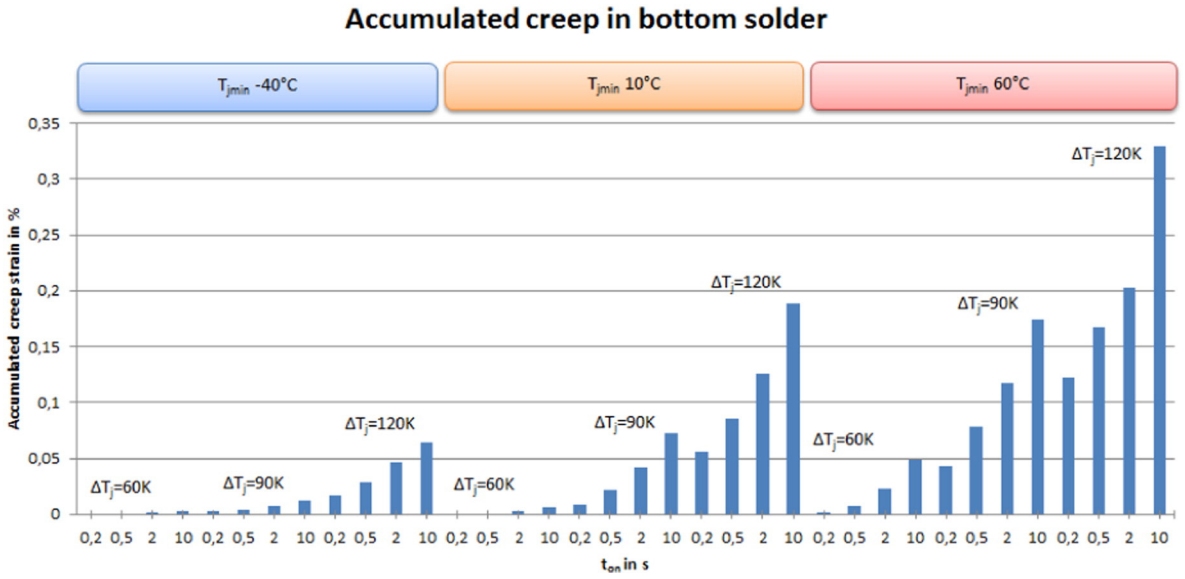


Fig. 13. Histogram showing the accumulated creep strain in the bottom solder for different sets of test parameters.

6. Sensitivity study

A sensitivity study of test parameters (T_{jmin}, ΔT_j, and t_{on}) was simulated and the influence of those parameters on accumulated creep strain component is quantified.

6.1. Bottom solder behavior

The accumulated creep strain in one cycle was taken as an indicator of solder degradation and is plotted for the bottom solder and for all cases of the sensitivity study on Fig. 13. Because creep is a time dependent plasticity occurring at high temperatures, results of the sensitivity study are logical: creep strain accumulates with high T_{jmin}, large ΔT_j and long t_{on}. Thus here, the worst case of APC occurs with $T_{jmin} = 60°C$, $\Delta T_j = 120K$ and $t_{on} = 10s$, and it leads to 0.33% of accumulated creep strain.

6.2. Top solder behavior

Results of the sensitivity study of test parameters on the accumulated creep strain in the top solder is plotted Fig. 14. As expected creep strain accumulates with high T_{jmin}, large ΔT_j and long t_{on}, but there are 4 cases of exception: cases with $T_{jmin} = 60°C$, $\Delta T_j = 120K$ and t_{on} ranging from 0.2s to 10s. These exceptional results may be explained by the fact that the mold has an influence on the creep behavior of the top solder. At $T_{jmin} = 60°C$ and with $\Delta T_j = 120K$, the glass transition temperature of the mold $T_g = 150°C$ is surpassed and therefore the Young's modulus of the mold drops down. This may induce some changes, at least numerically, in the behavior of the structure and leads to a decrease of creep strain in the top solder behavior. So, here the worst case is reached for $T_{jmin} = 60°C$, $\Delta T_j = 120K$ and $t_{on} = 0,2s$, with 0.99% of accumulated creep strain. The amount of accumulated

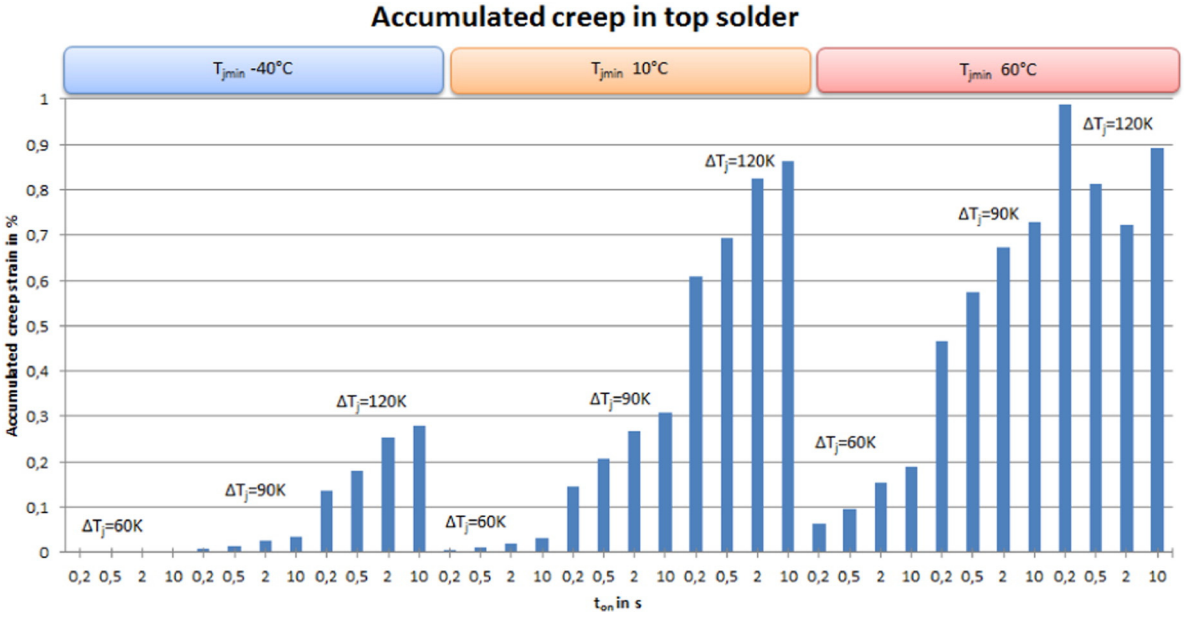


Fig. 14. Histogram showing the accumulated creep strain in the top solder for different sets of test parameters.

creep strain is a bit more than 3 times higher than what was accumulated in the bottom solder.

Confronting numerical and experimental results reveals that in the numerical sensitivity study creep strain is always accumulated in solder whatever the test parameters, whereas in experiments, no degradations were observed under the field load $\Delta T_j = 60K$, even after several millions of cycles. Results of the numerical sensitivity study are actually depending on the model defined to represent the solder behavior. Therefore real solder may behave differently than what is numerically predicted. Thus the question previously raised about the nature of the failure mechanisms occurring under $\Delta T_j = 60K$ and under $\Delta T_j = 90K$ or 120K still remains. One way to have more detailed information on mechanisms involved in solder degradation under APC would be to regularly monitor the Z_{th} of tested modules and to regularly analyze the microstructure of metallographic specimens.

Results of the sensitivity study can be summarized as follows in the Table 6. It presents the worst set of test parameters (T_{jmin}, ΔT_j and t_{on}) regarding creep strain in solder layers. Logically, both solder layers accumulate more creep strain with high T_{jmin}, large ΔT_j and long t_{on}.

7. Lifetime models

With the experimental APC tests, the solder lifetime can be predicted in function of different sets of test parameters. With the FEM simulations, amounts of creep strains accumulated in 1 cycle were calculated for different sets of test parameters. Combining the results obtained from both experiments and simulations, allow plotting a solder lifetime prediction diagram in function of the creep strain accumulated. Then a power trend line fitting the best the scattered points is determined. The trend line equation defines then the lifetime model like in the form of a Coffin Manson model:

$$N_f = a \quad (x)^{-b} \tag{3}$$

Where N_f is the number of cycles to failure, a a coefficient and b an exponent determined with experiments and x the percentage of accumulated creep strain in one cycle.

Then regarding the lifetime requirements under APC, these ones are strongly dependent on the application of the module. However, it can be roughly considered that with $\Delta T_j = 80$-90K, a lifetime of 100.000 cycles is a minimum required while a lifetime of 1 million of cycles characterized already a robust module. Here it is important to note that modules were submitted up to 2 million cycles and were always electrically functional at the end of tests.

7.1. Bottom solder behavior

A lifetime model for the bottom solder is defined by stating that the end-of-life is reached when an increase in Z_{th} superior to 10% [20], and/or some cracks were observed in the bottom solder at the end of test. The result is presented Fig. 15 and shows the lifetime prediction of the bottom solder in function of its accumulated creep strain. The determination of the trend line lacks of reliability due to a lack of data and of precision in the definition of the end of life. Indeed, for some cases the

Table 6
Recap chart of the worst sets of parameters for creep strain accumulation in solder layers.

	Inputs			
Outputs	of output parameters	T_{jmin}	ΔT_j	t_{on}
	Acc creep Bottom solder	↗	↗	↗
	Acc creep Top solder	↗	↗	↗

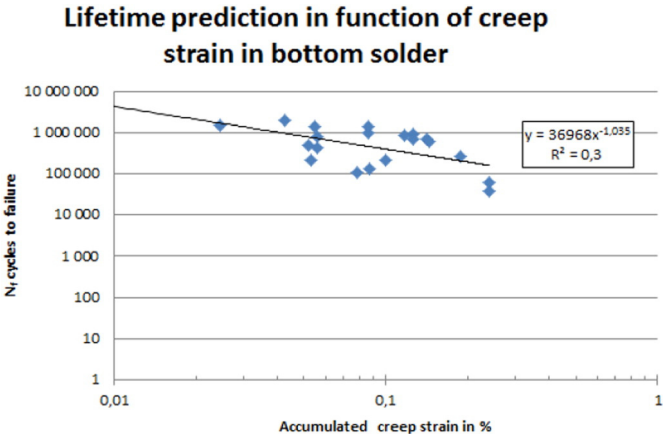


Fig. 15. N_f cycles to failure in function of the accumulated creep strain in the bottom solder.

Z_{th} was missing: a regular measure of it should have been planned for each tested sample to correctly follow the evolution of Z_{th} under APC. Then, the criterion based on the presence of cracks shows some uncertainties as it is a local and non-quantitative criterion. If the degraded surface was precisely measured for each sample a quantitative criterion based on the amount of degraded surface could have been defined. Because of this lack of precise data, the lifetime model was established taking the end of test as corresponding to the end-of-life.

But Fig. 15 still provides a first interesting approximation of the lifetime prediction.

For 0.02% the lowest value of accumulated creep strain a lifetime of 1.5 million of cycles can be expected whereas for 0.3% the highest amount of accumulated creep strain, the lifetime is divided by 24, leading to a lifetime of 62.000 cycles. This lifetime seems quite low, but was reached under severe loading condition with $\Delta T_j = 170K$. According to the lifetime model, a lifetime equal or superior to 500.000 cycles can be reached if the accumulated creep strain stays equal or inferior to 0.08%. Thus this 0.08% of accumulated creep strain could define a critical limit for the bottom solder lifetime.

7.2. Top solder behavior

For the determination of the top solder lifetime model, the method was approximately the same as for the bottom solder. The lifetime model was defined by stating that the end-of-life was reached when some cracks were observed in the top solder at the end of test. The resulting lifetime prediction is presented Fig. 16. Here also the determination of the trend line lacks of reliability due to a lack of data and of precision in the definition of the end of life. Indeed, here no electrical

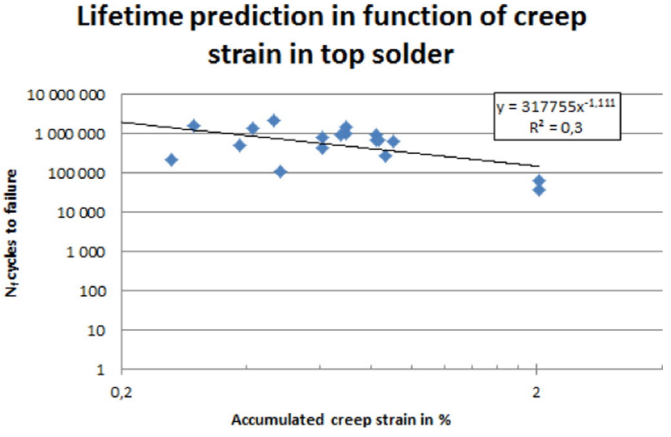


Fig. 16. N_f cycles to failure in function of the accumulated creep strain in the top solder.

or thermal parameter is indicating the degradation of the top solder layer. Moreover, as explained previously, the criterion based on the presence of cracks is only a local and non-quantitative criterion. But in the case of the top solder it is really difficult to obtain accurate measures of cracks or of its degraded surface. Thus the definition of a representative and quantitative criterion is not evident for the top solder. So here also, due to the lack of precise data, the end of test was taken as corresponding to the end-of-life. But Fig. 16 still gives a first idea on lifetime expectations.

For 0.3% the lowest value of accumulated creep strain a lifetime of 1,5 million of cycles can be expected whereas for 2% the highest amount of accumulated creep strain, the lifetime is divided by 24, leading to a lifetime of 62.000 cycles. Just like for the bottom solder, this lifetime of 62.000 cycles appears to be low, but was reached under $\Delta T_j = 170K$. Thus, the top solder layer can also be considered as robust. According to the lifetime model, in order to have a lifetime equal or superior to 500.000 cycles, the accumulated creep strain has to stay equal or inferior to 0.65%.

So, it results from this study that for a defined lifetime, the top solder can accumulate a lot more creep strain than the bottom solder. This can be explained by several different mechanisms. First, the temperature in the top solder is always higher than in the bottom solder. Indeed, unlike the top solder, the bottom solder is on the thermal cooling path evacuating the heat generated by the chip to the heat sink. So, this higher temperature in the top solder results in a higher susceptibility to creep compared to the bottom solder. But, this high susceptibility to creep does not lead to a premature failure of the top solder. This is because other phenomena are involved in solder degradation: due to large CTE mismatch between joined layers and large spatial temperature gradients, the cyclic temperature shifts during operation can produce cyclic shear strain in solder joint, and this may lead to cracking of the joint. For the bottom solder, being located on the thermal cooling path between the heating source and the heat sink, leads to higher spatial temperature gradients than in the top solder. Moreover, the CTE mismatch between the Si chip (2.8) and the Cu lead frame (16.5) joined by the bottom solder, is larger than the CTE mismatch between the Cu clip (16.5) and the Al metallization (25.3) joined by the top solder. Thus, the large spatial temperature gradient and the large CTE mismatch between Si and Cu are making the bottom solder more susceptible to crack than the top solder. And in terms of solder degradation, this last mechanism may be dominant compared to creep mechanism, this leading to more important damage in the bottom solder compared to the top solder. Moreover, it is not critical for the module to cope with top solder damages, as unlike for the bottom solder, top solder degradations do not have electrical or thermal consequences.

8. Conclusion

Under power cycling, cracks are starting at the meniscus and propagate toward the center of the chip in the bottom solder. These degradations affect the thermal path and lead to an increase in the Zth curve. In the top solder, cracks are starting at the meniscus close to the interface with the chip or with the Cu clip and propagate toward the center of the clip. But top solder degradations do not have significant influences neither on electrical functionality nor on the thermal path of the device.

Finite Element simulations confirm that the meniscus area is critical in solder layers, as the maximum of creep strain is reached at that location. Based on the evaluation of accumulated creep strain at this critical area, a numerical sensitivity study on test parameters is conducted for the bottom and the top solder. High T_{jmin} with large temperature swings ΔT_j and long pulse width t_{on} are the most critical test parameters for both solder layers.

Finally, lifetime models for solders are defined by stating the end-of-life reached by an increase of 10% or more in Z_{th}, and/or the presence of important cracks in solder at the end of test. Lifetime models are then obtained by correlating the experimentally deduced solder lifetime with the corresponding calculated creep strain. It appears that damages in the top solder are less critical than damages in the bottom solder, as high amount of creep strain can be accumulated in the top solder and still not lead to a premature failure of the device. However, the bottom solder degradation does not seem to be critical as no systematical large increase in Z_{th} were reported for the APC tests. The understanding of the failure mechanisms in solder joints and the solder lifetime models could be further improved by carrying out more experiments with a regular monitoring of the Z_{th} and a systematic and precise measurement of the degraded surface in solder joints.

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